

# EIModule

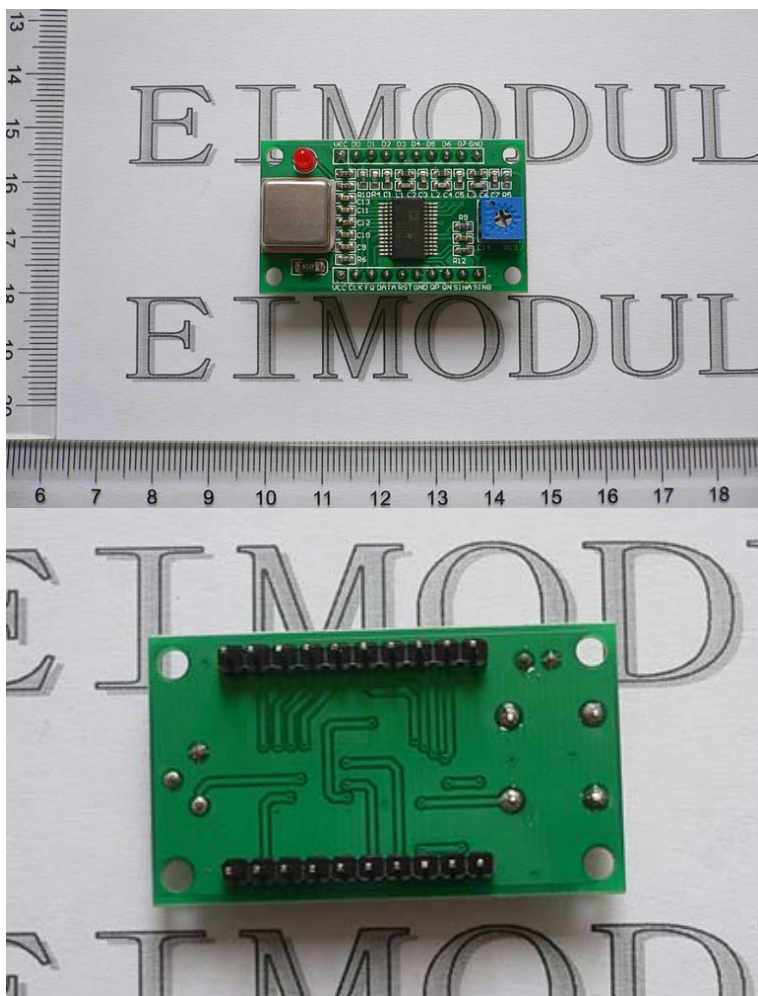
## ADS9850 Signal Generator Module

### 1. Introduction

This module described here is based on ADS9850, a CMOS, 125MHz, and Complete DDS Synthesizer.

The AD9850 is a highly integrated device that uses advanced DDS technology coupled with an internal high speed, high performance, D/A converter and comparator, to form a complete digitally programmable frequency synthesizer and clock generator function.

All the external components which are needed are integrated on the board and the designer don't need to care more about the detailed design of ADS9850. The designer only needs to add the power and control signals to this module to driver this module



<http://www.eimodule.com>

# EIModule

## 2. FEATURES and APPLICATIONS

### 2.1 FEATURES:

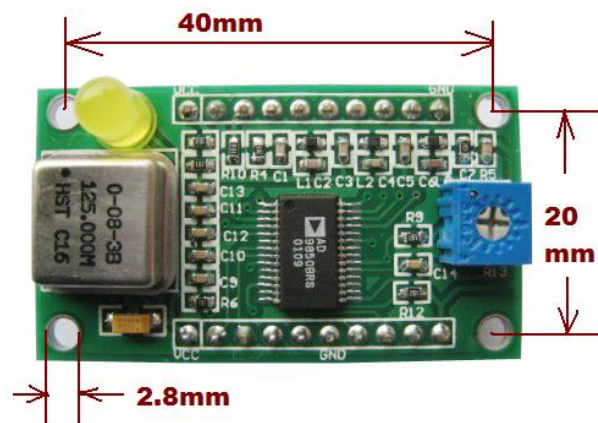
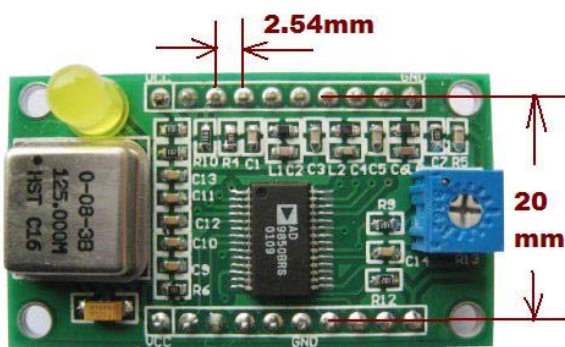
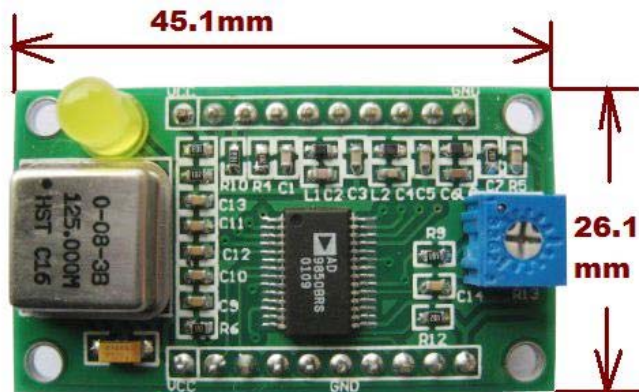
- **Signal Frequency output range: 0-40MHz**
- **4 Signal outputs:**
  - 2 sine wave outputs and 2 square wave outputs**
- **DAC SFDR > 50 dB @ 40 MHz AOUT**
- **32-Bit Frequency Tuning Word**
- **Simplified Control Interface: Parallel Byte or Serial Loading Format**
- **Phase Modulation Capability**
- **+3.3 V or +5 V Single Supply Operation**
- **Low Power: 380 mW @ 125 MHz (+5 V)**
- **Low Power: 155 mW @ 110 MHz (+3.3 V)**
- **Power-Down Function**

### 2.2 APPLICATIONS

- **Frequency/Phase–Agile Sine-Wave Synthesis**
- **Clock Recovery and Locking Circuitry for Digital**
- **Communications**
- **Digitally Controlled ADC Encode Generator**
- **Agile Local Oscillator Applications**

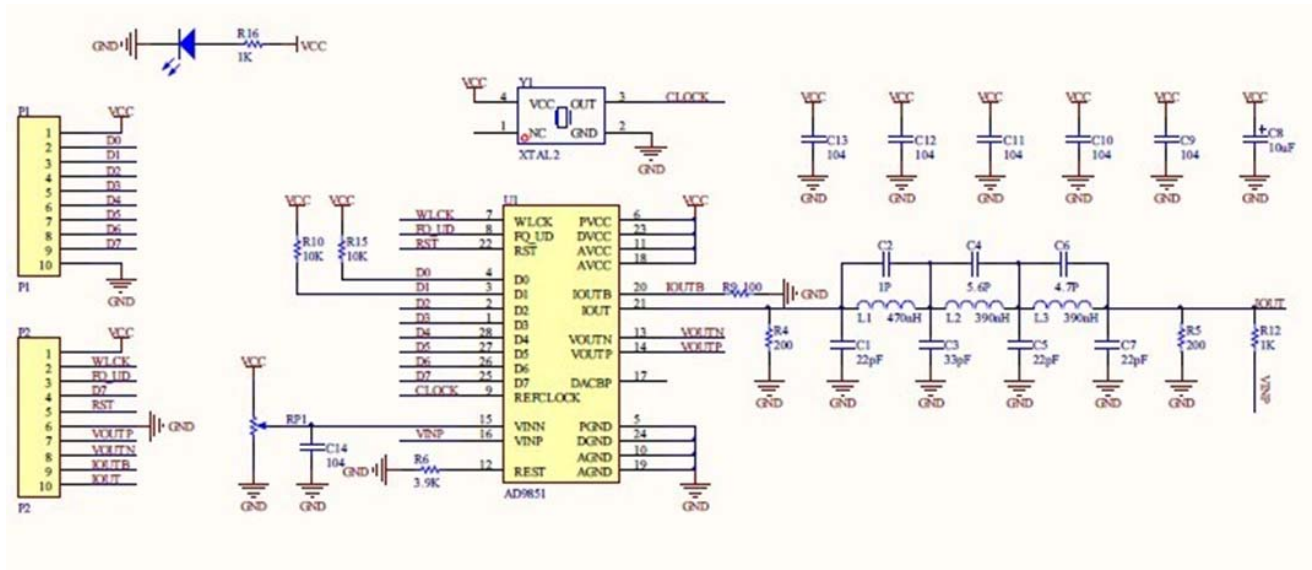
# EIModule

## 3. The assembly drawing



# EIModule

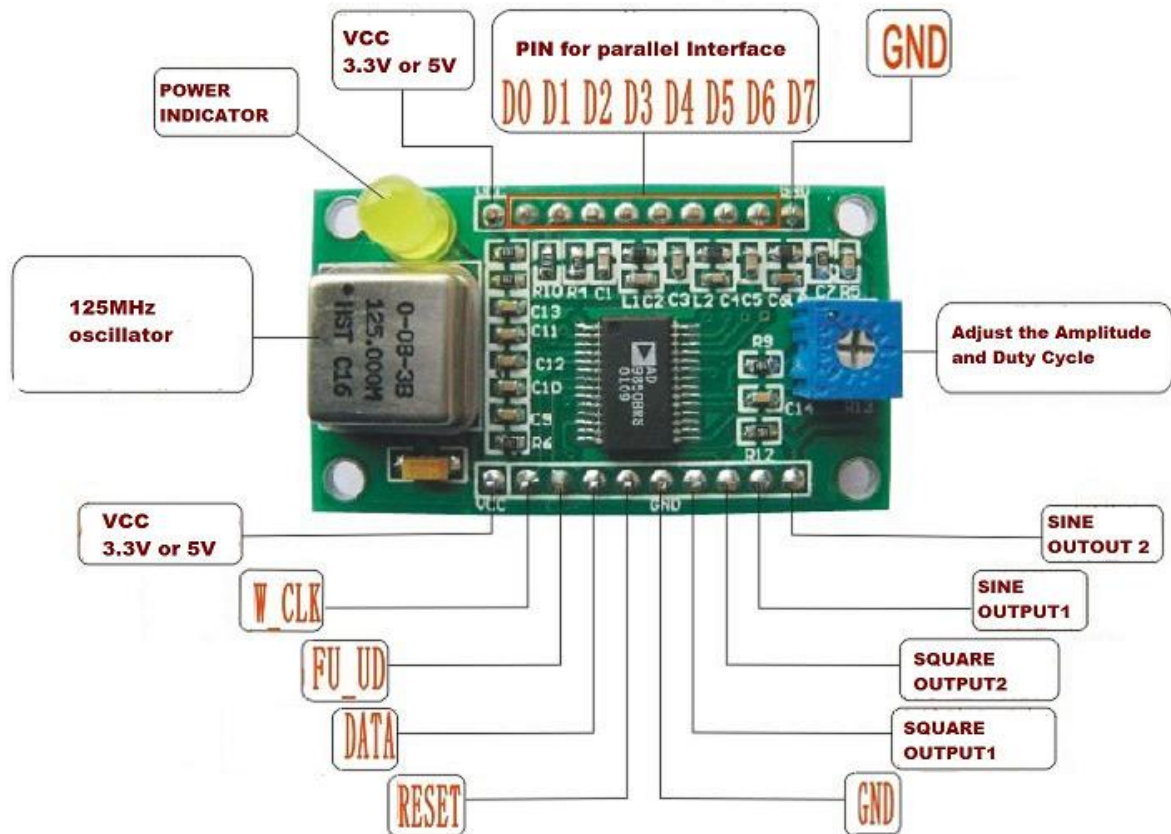
## 4. Schematic



# EIModule

## 4. How to drive this module

### 1) Pin definition



Symbol	Type	Function
VCC	P	This is a voltage supply pin. 3.3V or 5V power input
GND	P	This is a ground pin.
W_CLK	I	Word Load Clock. This clock is used to load the parallel or serial frequency/phase/control words
FQ_UD	I	Frequency Update. On the rising edge of this clock, the DDS will update to the frequency (or phase) loaded in the data input register, it then resets the pointer to Word 0
DATA	I	D7, Serial Load
RESET	I	Reset. This is the master reset function; when set high it clears all registers (except the input register) and

<http://www.eimodule.com>

# EIModule

		the DAC output will go to Cosine 0 after additional clock cycles
D0–D7	I	8-Bit Data Input. This is the 8-bit data port for iteratively loading the 32-bit frequency and 8-bit phase/28–25 control word. D7 = MSB; D0 = LSB. D7 (Pin 25) also serves as the input pin for the 40-bit serial data word.
Square Wave Output1	O	This is the comparator's true output
Square Wave Output1	O	This is the comparator's complement output.
Sine Wave Output1	O	Analog Current Output of the DAC.
Sine Wave Output1	O	The Complementary Analog Output of the DAC.

## 2) DC Characteristics

- 1) Power supply: 3.3V or 5.0V
- 2) Interface voltage: 3.3V if power supply is 3.3V.  
5.0V if power supply is 5.0V

Characteristics	Symbol	Min	Typ	Max	Unit
Logic "1" Voltage +5 V Supply	$V_{IH}$	3.5	5.0	6	V
Logic "1" Voltage +3.3 V Supply	$V_{IH}$	3.0	3.3	6	V
Logic "0" Voltage	$V_{IL}$		-	0.4	V



# EIModule

## 3) Software description

The AD9850 contains a 40-bit register that is used to program the 32-bit frequency control word, the 5-bit phase modulation word and the power-down function. This register can be loaded in a parallel or serial mode.

In the parallel load mode, the register is loaded via an 8-bit bus; the full 40-bit word requires five iterations of the 8-bit word. The W\_CLK and FQ\_UD signals are used to address and load the registers. The rising edge of FQ\_UD loads the (up to) 40-bit control data word into the device and resets the address pointer to the first register. Subsequent W\_CLK rising edges load the 8-bit data on words [7:0] and move the pointer to the next register. After five loads, W\_CLK edges are ignored until either a reset or an FQ\_UD rising edge resets the address pointer to the first register.

In serial load mode, subsequent rising edges of W\_CLK shift the 1-bit data on Lead 25 (D7) through the 40 bits of programming information. After 40 bits are shifted through, an FQ\_UD pulse is required to update the output frequency (or phase).

For detailed information for Programming the AD9850, please download the following two documents on our website: [www.eimodule.com](http://www.eimodule.com) (Search EIM377)

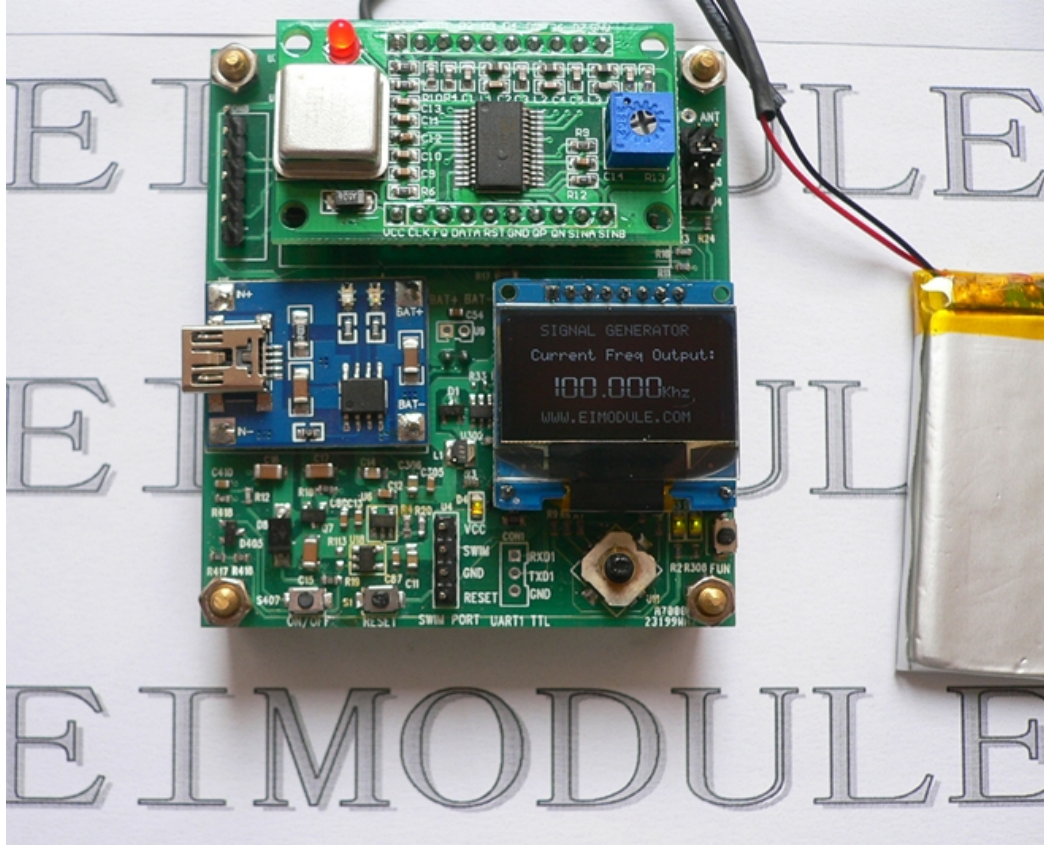
1. AD9850\_specification.pdf (From Page 9)
2. AD9850\_SW\_samples.zip

We also have demo board for this module for you. See the picture on the next page.

<http://www.eimodule.com>

# EIModule

## 5. Pictures for working module



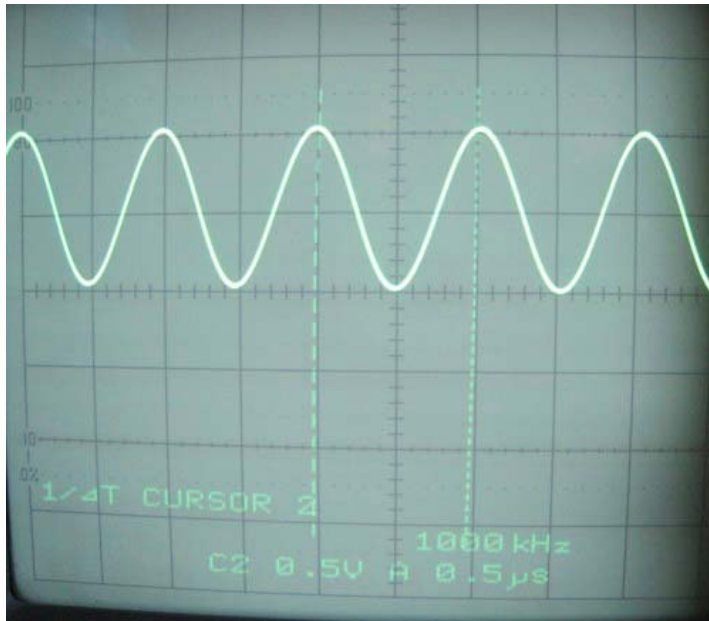
<http://www.eimodule.com>



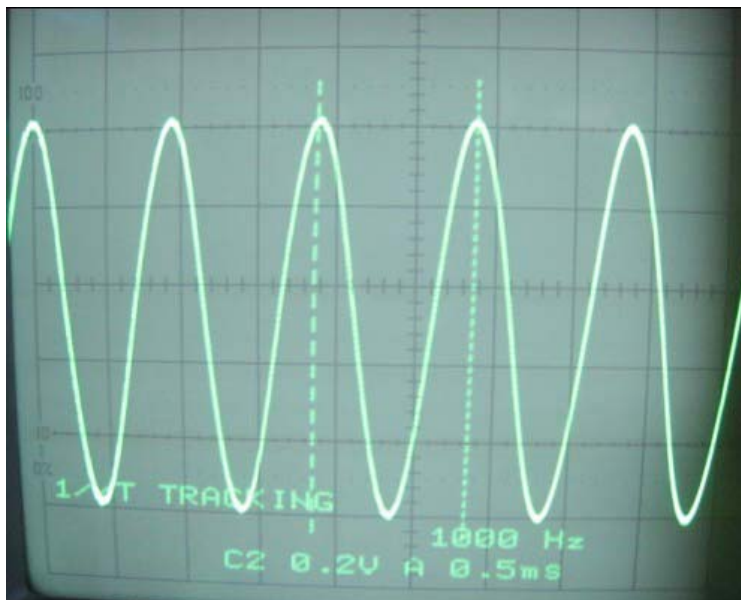
# EIModule

## 6. Test results

1MHZ 正弦波输出图:



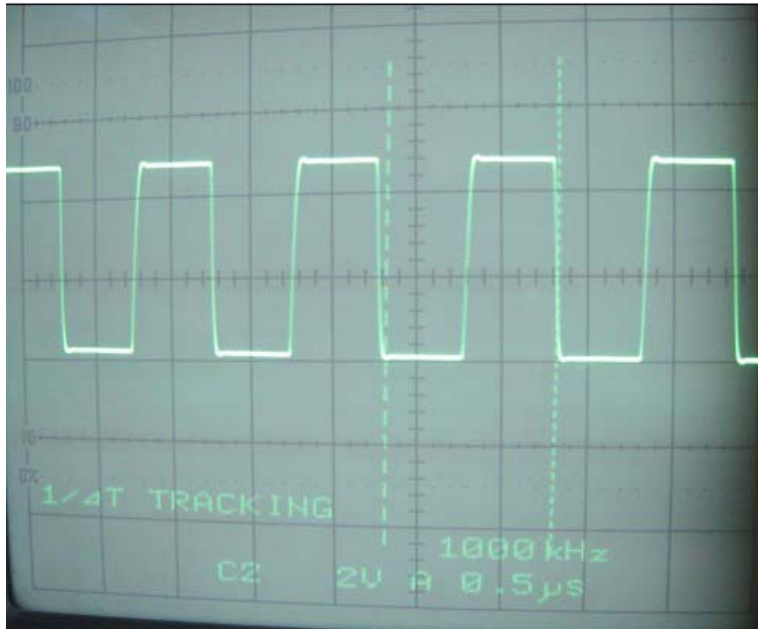
1KHZ 正弦波输出图:



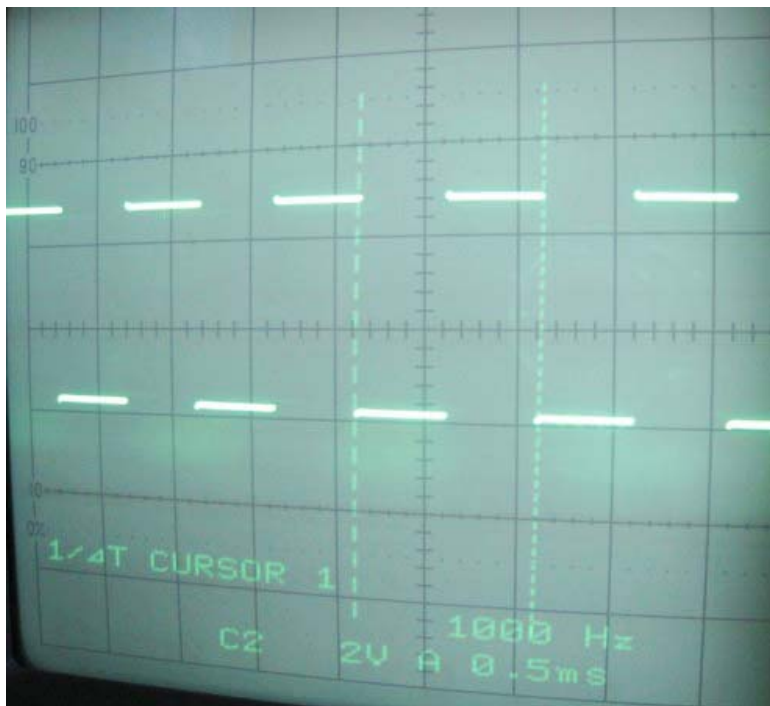
<http://www.eimodule.com>

# EIModule

1MHZ 方波输出图:



1KHZ 方波输出图:



<http://www.eimodule.com>