PmodGYRO Demo Project

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Overview

This document presents Verilog implementation details to interface the PmodGYRO. The project first configures the PmodGYRO, and then begins to sample temperature and axis data at 100Hz. The user uses switches on the Nexys3 to select which data they want to display on the seven segment display. The selected data is continuously sampled and displayed on the seven segment display (SSD) when active. For data selection details see Table 1 below. For I/O pin descriptions see Table 2 on page 3. The PmodGYRO connects to port "JA" on the Nexys3.

Table 1 – Display Data Selection

SW3	SW2	SSD Output
Off	Off	x-axis
Off	On	y-axis
On	Off	z-axis
On	On	Temperature

Functional Description

Figure 1 to the right shows a block diagram of the PmodGYRO Demo. There are three main components in this demo, master_interface, spi_interface, and display_controller. Switch *SW1* on the Nexys3 is used as a *start* signal.

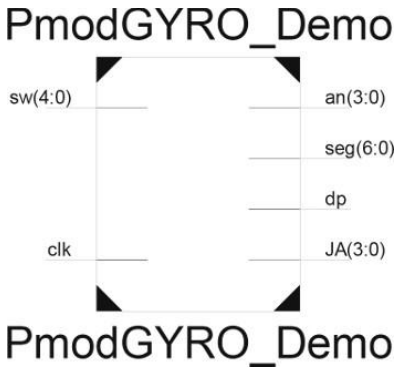

Fig. 1 – PmodGYRO Demo

The master_interface component receives the status of *SW1* on its *start* input, and is used to initialize a data transfer between the PmodGYRO and the Nexys3. Once a *start* signal is received, a configuration byte is output by the master_interface on its *send_data* output bus. The *begin_transmission* output of master_interface is used to initialize a byte transfer with the PmodGYRO.

When the spi_interface component receives a *begin_transmission* signal, it stores the data on its *send_data* input, and transmits the data to the PmodGYRO. As the spi_interface transmits a byte of data, it reads a byte of data, and outputs the received data on its *received_data* output bus. Once a data byte has been transmitted the spi_interface component handshakes with the master_interface component by asserting its *end_transmission* output. SPI mode 3 is used for data transmission in this design.

When master_interface receives a handshake it stores the received data, and configures the next byte of data to be transmitted. Received data is made available to the rest of the design on the *temp*, *xAxis*, *yAxis*, and *zAxis* outputs of master_interface. These outputs are then sent into the display_controller component with the status of switches SW4, SW3, and SW2 on the Nexys3. Switch SW4 is used to select between displaying data in hexadecimal or decimal format. Depending on the configuration of switches SW3 and SW2 (*see Table 1 above*), either the temperature data or one of the axes data, will be displayed on the seven segment display.

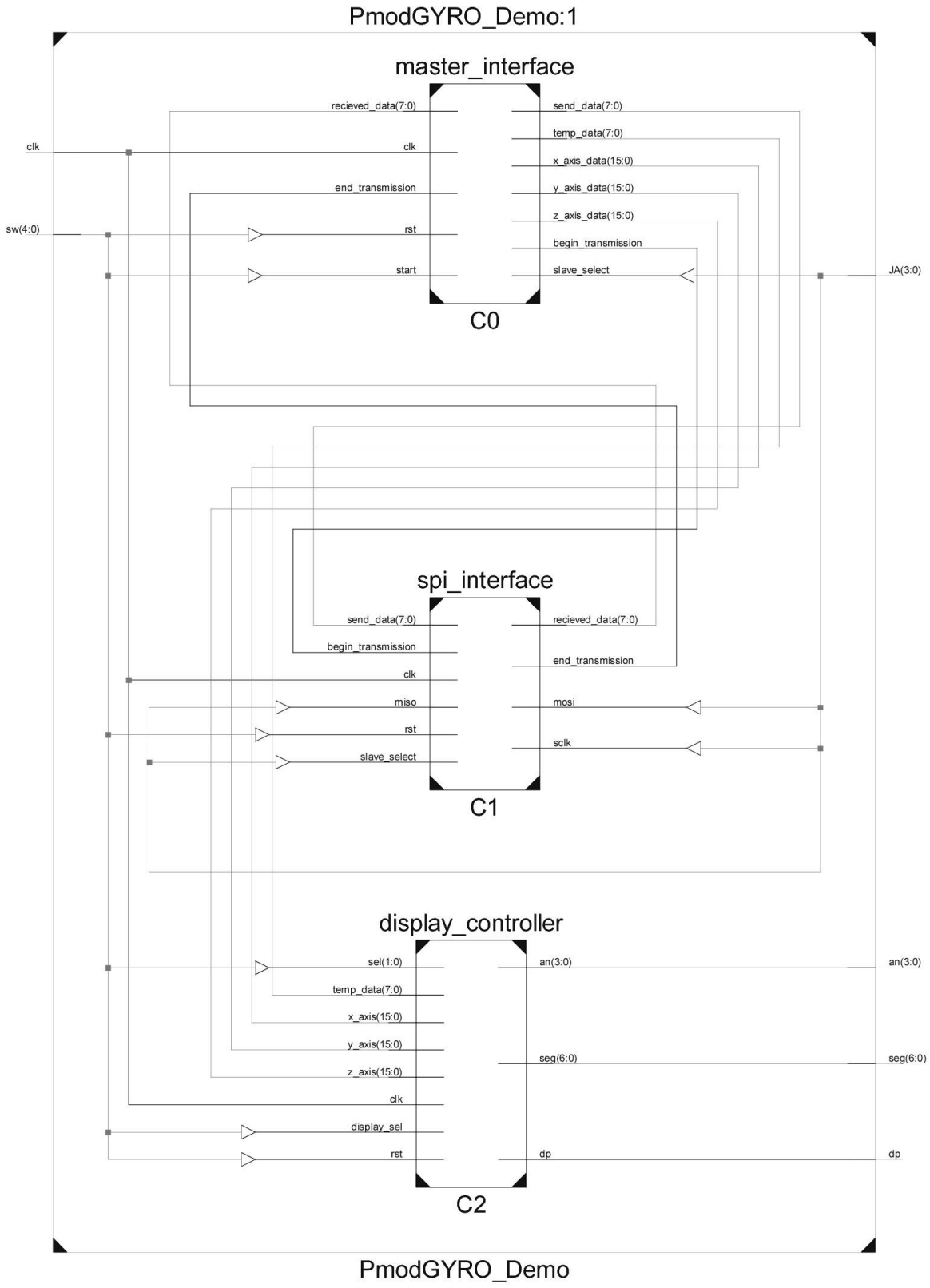

Fig. 2 – PmodGYRO Demo Interconnections

Table 2: Input/Output Pin Description	
Signal	**Description**
CLK	Input clock, 100MHz onboard fixed oscillator.
SW(4:0)	Input switches for selecting temperature or axis data to display on SSD, etc.
AN(3:0)	Output anodes for controlling illumination of SSD digits.
SEG(6:0)	Output cathodes for displaying digits on SSD.
DP	Output cathode for displaying decimal place on SSD.
JA(3:0)	Inputs/Outputs for SPI communication with PmodGYRO

Component Description

display_controller

This component receives data from the master_interface component, formats the data, and produces the necessary output signals to display the data on the SSD. This component uses the status of the onboard switches to select which data should be displayed on the SSD. For details on data selection see Table 1 on page 1.

master_interface

This module controls the data transmitted to the PmodGYRO and guides the data transmission process. The *rst* input forces the system into an idle state with standard starting values, and is tied to SW0 on the Nexys3. When the switch is asserted the demo will reset to starting conditions. The *start* input is used to initialize a data transfer with the PmodGYRO. It should be noted that data cannot be sampled until the PmodGYRO has been properly configured first.

Once a *start* signal is received, the PmodGYRO is immediately configured to output data at a rate of 100 Hz with 8.75 mdps/digit at 250 dps maximum. Data will be sampled continuously until *start* is no longer asserted.

This component uses the onboard 100 MHz clock of the Nexys3, and updates on rising edges. The *begin_transmission* and *end_transmission* signals are used for handshaking between the *master_interface and spi_interface* components. The begin_*transmission* signal indicates the beginning of a transmission to the PmodGYRO, and the end_transmission signal indicates that the *spi_interface* has completed data reception of a byte from the PmodGYRO.

spi_interface

This component receives and transmits data and produces the 12.2 kHz *sclk* , which drives communication with the PmodGYRO. When master_interface asserts its *begin_transmit* output, the value on the *send_data* input bus is moved into a shift register and is shifted out during transmission. As data is shifted out, data is shifted into the *received_data* register. The *received_data* is output to the *received_data* input bus on the master_interface component. Once transmission and reception of a byte has completed, spi_interface handshakes with master_interface by asserting its end_transmission output.